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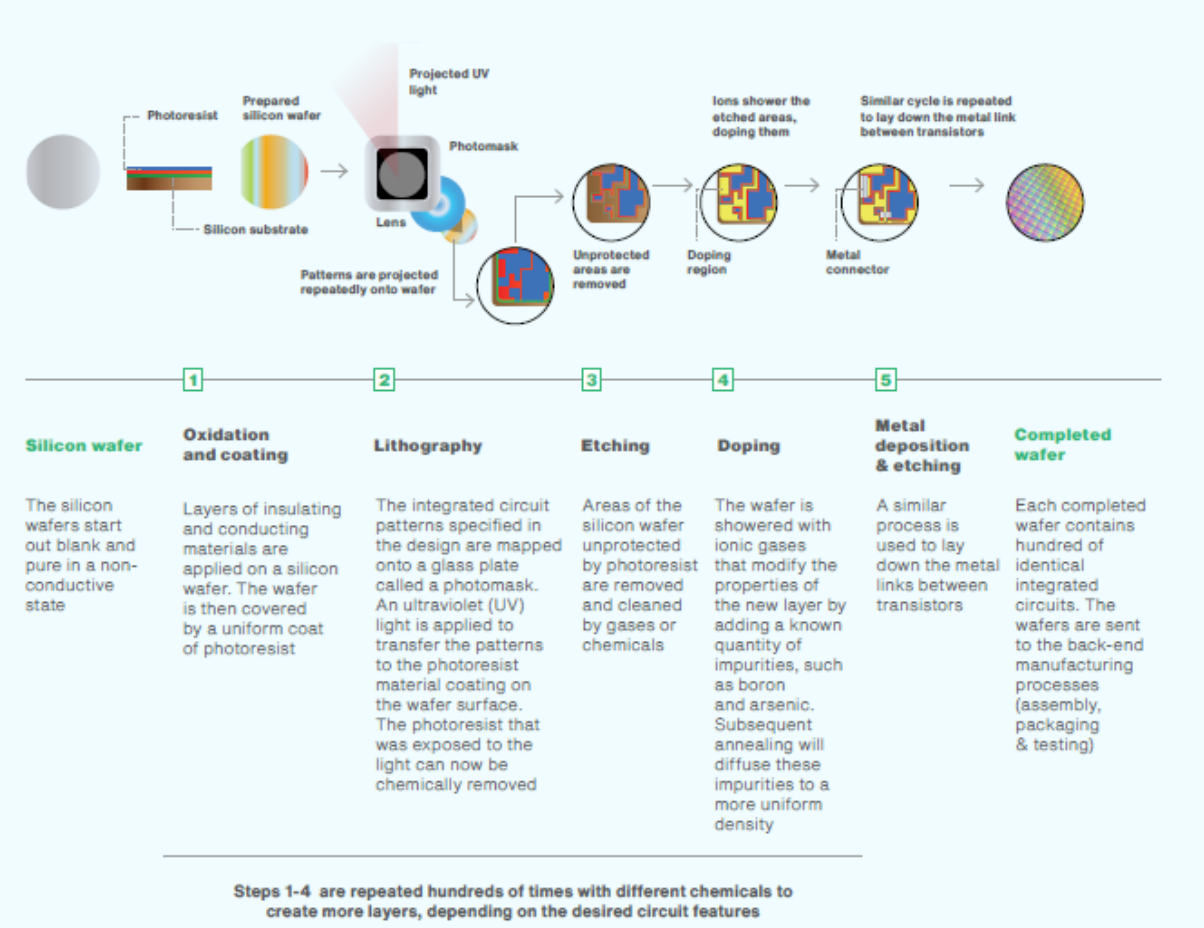
PART 4/4

# COMMISSION STAFF WORKING DOCUMENT

## A Chips Act for Europe

# Annex 2. Semiconductor Manufacturing Steps

The main steps in the chip manufacturing process are set out in the following schematic[1]:




The key feature of the manufacturing process is that all the transistors on all the die[2] on the wafer are created simultaneously, and each layer of metal is created simultaneously across the whole wafer. It is this incredible level of efficiency, making trillions of transistors at once, that has allowed the price of electronic products to fall by around 5% per month, year after year.

It is worth emphasizing that the manufacturing process doesn't depend on what is being manufactured. A computer printer does not need to be reconfigured depending on what you want to print, you just send it different data. In the same way, a semiconductor manufacturing process doesn't depend on what the circuit is going to do.

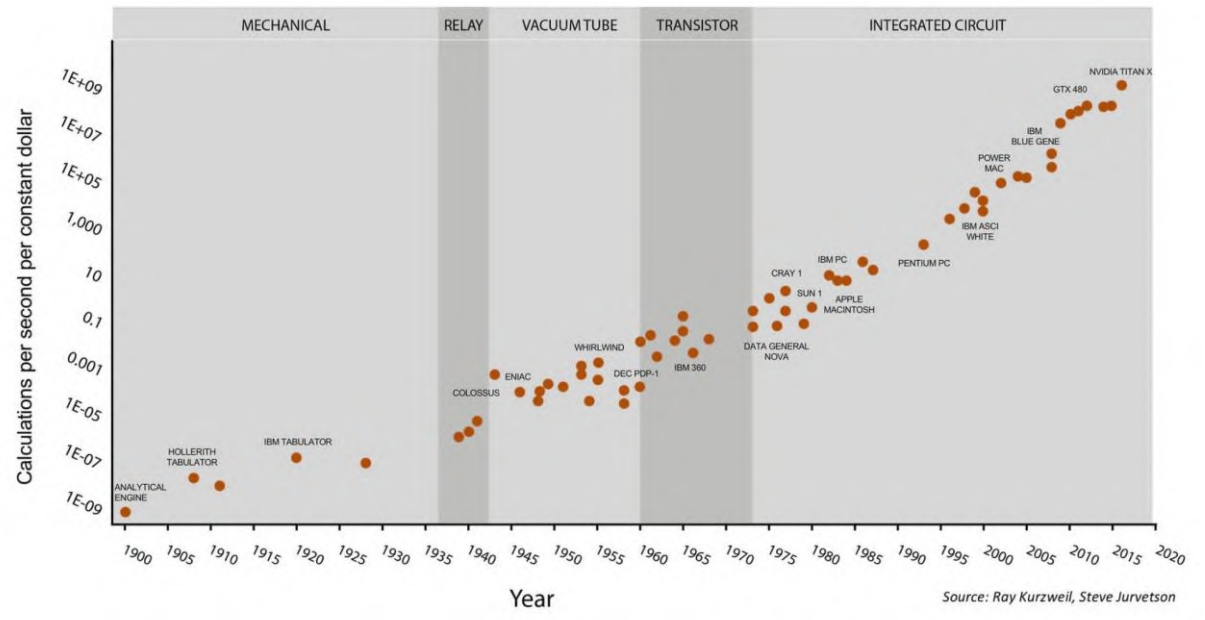
The fab where chips are manufactured are kept very clean - the air may be completely changed every few seconds, as particulate filters in the ceiling blow air down and out through perforations in the floor before being filtered and recirculated. Recently, fabs have found that even that air is not clean enough. A few random particles landing on a die can ruin it. These days, the wafers being processed are contained in even cleaner boxes that attach to each piece of manufacturing equipment in turn. A

[1] BCG x SIA, "Strengthening the global semiconductor supply chain in an uncertain era", April 2021.
[2] The die refer to the parts of the wafer on to which each chip is fabricated.

large part of the cost of a fab is not the manufacturing equipment, expensive though it is, but the equipment for keeping everything inside the fab clean.

Why is cleanliness so important? The transistors on a modern chip are some few nanometres (nm) across. By contrast, a human hair is around 100,000 nm. Obviously, a hair ending up on a wafer would be a complete disaster, blocking thousands of transistors from being manufactured correctly and causing that die to fail. But it only takes something around 10 nm across to on the wafer to cause a die to (probably) fail. If a die is not manufactured correctly, it is simply thrown away. There is typically no repair process to fix it after it's made.

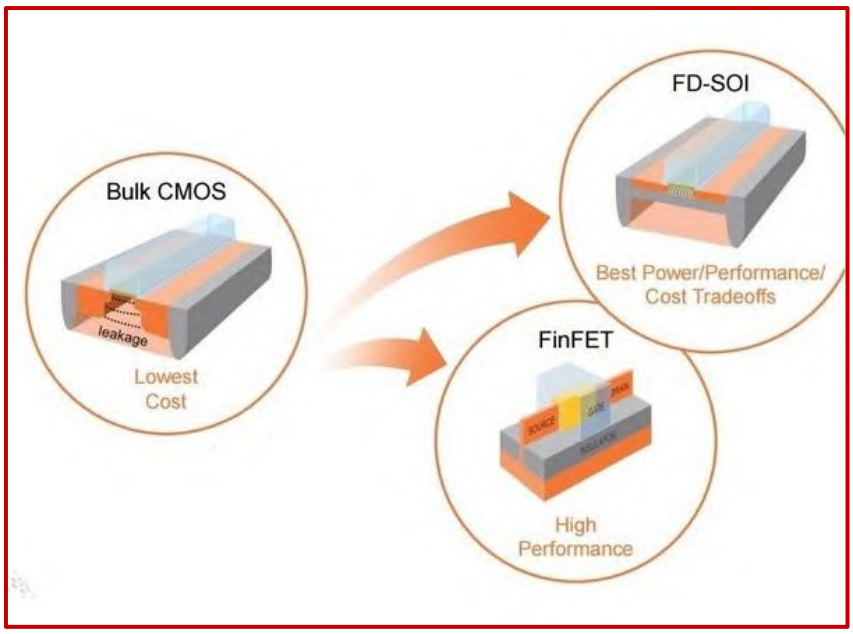
# Annex 3. Moore’s Law




One famous representation of the processor industry is Moore's Law. This describes how the number of transistors in a chip doubles roughly every 18 months. This was true for a very long time, but is starting to slow down. Transistors are getting so small that we are nearing the limit of what physics will allow.

# Annex 4. FinFET and FDSOI Semiconductor Technologies

Since the 1960s, the business of chip production has been driven by **doubling the number of transistors in a given area of semiconductor** and **hence doubling the computing power every eighteen months** (Moore's law). Complying with Moore's law requires **shrinking the feature size**[3] (28nm, 22nm, 16nm, 12nm, …)[4], increasing the wafer size (200 mm, 300 mm, …), or building vertically onto the chip (shifting from 2D to 3D architectures).




A major target in chip design and fabrication is to reduce and control the current - which activates the transistor gate[5] - and accordingly, the performance of the chip (switching speed & power consumption).

However, as transistors shrink, so does the proximity between its constituent components (the gate, source and drain). This gives rise to undesirable physical effects including loss of the gate's ability to control the current.

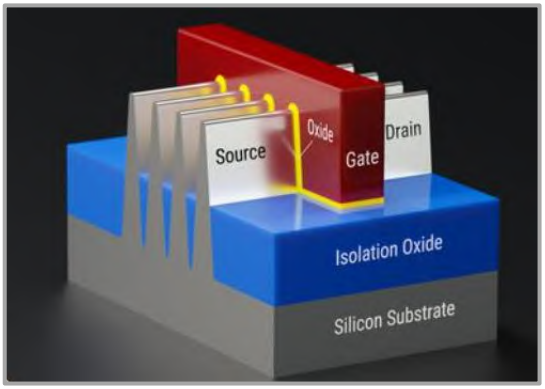
At process nodes below 28nm, transistors produced with conventional bulk CMOS technology no longer work because of these physical effects. This led to the development of alternative technologies, the most commonly used today being **FinFET** (fin field-effect transistor) and **FD-SOI** (fully depleted silicon on insulator), with **FinFET being the main technology of choice**.

These technologies differ in their **physical architecture,** which has a bearing on the respective fabrication processes. They also exhibit different **performance** characteristics, which will determine their suitability for a specific final application.

**FinFET**

A FinFET is a non-planar transistor where the gate is a fork-shaped 3D structure similar to a fish "fin" as shown in the figure. This architecture greatly improves the control of the gate over the current and thereby the switching of the transistor from on to off. FinFET requires a more complicated manufacturing process than conventional bulk CMOS with many more process steps needed to achieve the 3D structure.

[3] In semiconductor manufacturing, the process technology (or process node) determines the dimensions at which transistors can be printed onto a silicon wafer. Smaller process nodes produce smaller transistors; the smaller the transistors, the more you can fit on a chip and the faster and more efficient your processor can be.
[4] 1nm or 1 nanometre = 1 billionth of a metre.
[5] The gate switches the transistor on or off. A voltage applied to the gate controls the conductivity, and thereby the flow of current, between the source and the drain.

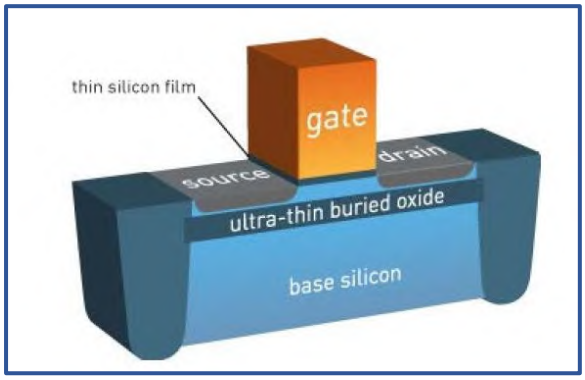



Chips utilizing FinFET have been on the market since the first half of the 2010s with Intel commercializing 22nm FinFET in 2011. With continuous optimization of the transistor density per chip, it has become the dominant design at 14nm, 10nm, 7nm and 5nm process nodes. The state of the art in FinFET is nominally 5 nm today, produced by TSMC and Samsung, with 3 nm in pre-production. Although European companies design in FinFET, they rely on foundries such as TSMC and Samsung for production.

FinFET devices are characterized by **fast switching speeds** and can support **high current densities** (present in heavily loaded circuits that operate 24/7).

**FD-SOI**

FD-SOI technology uses an ultra-thin layer of insulator positioned on top of the silicon substrate and a very thin silicon film as a means to better control the transistor behaviour. The architecture also enables the switching speed to be modulated dynamically during operation; this is a powerful means of optimizing power consumption when speed is less critical. Due to its planar structure, FD- SOI manufacturing is less complex requiring fewer process steps than FinFET.




Despite more costly[6] raw wafers (4 times more at around $400 rather than $100), the processed wafers are cheaper (some 7.3% lower for 14nm FD-SOI than for 16/14nm FinFET).

The simpler manufacturing process also makes it easier to add functionalities such as memory. The combination of memory and logic operations in a single process is attractive for applications at the edge of the network, including embedded AI in automotive and industrial manufacturing.

Currently, FD-SOI is in production at 28nm and 22nm (state of the art). Samsung has announced an 18nm node for which first production is expected in 2022. GlobalFoundries (GF) is developing 12nm FD-SOI at Dresden; it will be production ready in 2023-24.

FD-SOI exhibits excellent performance in terms of its behaviour at **radio frequencies (RF)** and its **reduced power consumption**.

**Advantages and disadvantages**

Both technologies have pros and cons and one may be inherently better than the other, **depending on the type of performance and requirements a specific application, product or system needs (speed, power consumption or cost)**.

[6] Due to the requirement that the silicon film and layer of insulator (buried oxide) need to be very thin and extremely uniform.

FD-SOI exhibits substantially reduced power consumption and is especially useful in lightly loaded circuits, like in IoT and portable/mobile applications, including automotive, where it enables longer battery life. Its RF variant, RFSOI, is used extensively in front-end modules (the interface between the transceiver and antenna) in smart phones and 4G/5G base stations.

FinFET will continue to be the technology of choice for applications with a lot of digital logic and that require the highest possible performance, like for HPC and supercomputing.

| | **FinFET** | **FD-SOI** | |
|---|---|---|---|
| Base wafer cost | | x4 | SOI wafer cost ca. $400 compared to bulk Si $100, but finished wafer ca. $5000 |
| Process complexity | ↑ | ↓ | FinFET ca. 40% more masks and process steps than FD-SOI |
| Overall/final wafer cost | → to ↗ | → to ↘ | finished wafer cost of 14nm FD SOI is 7.3% lower than that of 16/14nm FinFETs |
| Die yields | → to ↘ | → to ↗ | Yields higher with FD-SOI as bulk doping variability not an issue |
| Process control challenges | ↑ | ↓ | FinFET more complex |
| Transistor area density | ↑ | ↓ | Planar devices take more area |
| Performance/characteristics/cost | Higher performance, higher cost | Lower power, RF, lower cost | gate cost[7] for 14nm FD-SOI projected 16.6% lower than for 16/14nm FinFET |

However, FD- SOI is well suited to achieving a **better performance / power consumption trade-off at functionally equivalent nodes.**[8] It is fair to say that the two technologies compete in many applications including automotive, AI, IoT, 5G/6G, and industrial manufacturing.

**Developments**

FD-SOI process technology has been developed and industrialized in Europe by CEA Leti, STMicroelectronics (ST) and Soitec in 28nm. These developments received significant support from

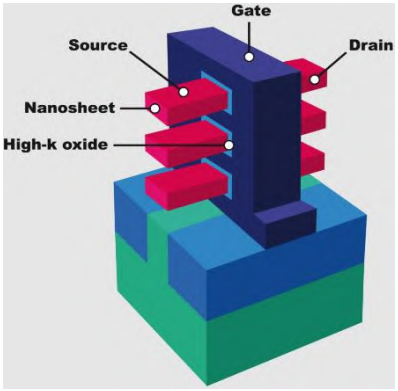
[7] The key cost factor for a customer is the "gate cost", a combination of the wafer cost, chip size and product yield.
[8] The 22nm FD- SOI technology exhibits similar performance to 14nm FinFET, with a lower production cost and researchers expect that 10nm FD-SOI will "likely" demonstrate similar performance to 7nm FinFET.

the predecessor Joint Undertakings to KDT (ECSEL and ENIAC). Samsung and GF have licensed the technology. There is a sizeable ecosystem in Europe that includes user companies such as NXP, Greenwaves, Valeo, Bosch and others as well as Racyics and Dolphin offering design services.

GF runs 22nm FD- SOI manufacturing lines in Dresden where it is also developing 12nm FD-SOI. The process has still to be optimized and will be production ready in 2023-24. Samsung has announced an 18nm FD- SOI node – for which first production is expected in 2022 - that might be a bridge to improved performance for customers using the 28nm node today. ST intends to license the 18nm technology from Samsung, integrate and further enhance it at Crolles. Such steps appear to be critical in enabling a route to 12/10nm nodes.

Scaling down FD- SOI technology to 10nm is expected to lead to significant improvements of chip performance compared to 22nm in terms of transistor density, power consumption, speed and RF behaviour. Transistor density can be improved by a factor of three and power consumption by a factor of two according to CEA-Leti. Research has shown that 10nm FDSOI will likely demonstrate similar performances in terms of transistor density, power consumption and speed to more advanced FinFET nodes such as 7nm, while maintaining its strong advantages for RF applications.

This would address the needs of a large part of the industrial market in Europe in the 2025-2027 time horizon, for example, for high-volume products like micro-controller units in the automotive and manufacturing industries as well as emerging markets in AI and communications.




While the path to 7nm FD-SOI is being *explored* in research settings - meaning there is *still much R&D work* to be done - 7nm and 5nm FinFET are already at volume production at TSMC and Samsung. 3nm FinFET is expected to reach mass production at TSMC in 2022 which is probably the limit for this architecture. Gate-All-Around Field-Effect Transistors (GAA-FET) - an evolutionary step from FinFET technology - will provide even better control of the gate over the current that is needed at these dimensions. TSMC is expected to release 2nm GAA-FET in 2023[9].

FinFET is without doubt a more mature technology than FDSOI, with scalability to lower node dimensions having been proven at industrial level. The equivalent scaling potential of FD-SOI has yet to be proven at volume production when it comes to node dimensions below 7nm.

[9] Samsung will use GAA-FET (nanosheet) also for 3nm - expected to be on track by 2022 for internal use (Samsung products) and made available to users through the company external foundry service in 2023.

# Annex 5. Examples of ongoing Pilot Lines in EU

**More-Moore Pilot Line**

- Development of proprietary Extreme Ultra Violet (EUV) lithography equipment for sub 10nm nodes,
- Development of adapted Metrology technology for those nodes including failure analysis,
- Development of EUV mask technology,
- Development of process modules (lithography, etching, deposition, etc.) with eventual tool development) for sub 10nm nodes in mostly FinFET technology for the 3nm and 2nm research was also done on new device geometries.

**FD-SOI Pilot Line**

- Development and demonstration in an industrial environment of the Full Deplete technology on a SoI (Silicon on Insulator substrate) including
- Demonstration that FD/RF SOI is suited for ultra-low-power IoT[10] automotive, edge AI and 5G-6G devices.
- Demonstration that the higher wafer cost is offset by the simpler processing of the component, at a targeted low-power, ensuring the value and competitiveness of SOI technology for the related applications.
- The practical validation that back biasing enables clear gains for battery-powered applications, e.g. mobile computing.
- The complementary embedding of non-volatile memory
- The demonstration that RFSOI is a versatile solution that enables 5G front-end for frequency range beyond 6GHz, through the integration of switches as well as amplifiers on the same silicon substrates. This concept is in production in Europe on 200 mm wafer substrates[11].
- The demonstration of the SOI competitive advantage in higher frequencies (over 120GHz) on radar for automotive applications, which cannot be done with any other technology.
- The development of a rich ecosystem of design companies and end users, enabling the expansion of a strategic technology to maintain the European autonomy and leadership in relevant sectors, e.g. automotive, 5G/mobile communications, AI, IoT.

**Pilot Lines for Heterogeneous Integration[12]**

ECSEL supported many projects at different TRL levels in the domain of heterogenous integration, some pilot line projects are discussed below:

**IoSense[13]** consists of three interconnected semiconductor pilot lines in Europe: two 200mm frontend lines (Dresden and Regensburg) and one backend (Regensburg) line. This allowed to increase the manufacturing capacity of sensor/MEMS components by a factor of 10 while reducing manufacturing

[10] Internet of Things
[11] SRIA 2021, page 41
[12] According to the "Heterogeneous Integration Roadmap" by the IEEE Electronics Packaging Society (https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2021-edition.html), heterogeneous Integration refers to the integration of separately manufactured components into a higher-level assembly (System in Package – SiP) that, in the aggregate, provides enhanced functionality and improved operating characteristics.
[13] http://www.iosense.eu/

cost and time by 30%. The time for idea-to market for new sensor systems was brought down to less than one year.

**MICROPRINCE**[14] has created the first worldwide open access foundry pilot line for micro-transfer-printing (μTP) and demonstrated its capability for heterogeneous integration of different functional components in an industrial environment. Hence, cheaper and more miniaturized photonic integrated sensors systems could be fabricated based on the μTP process which will enable new medical diagnostic systems. This project is a nice example as to how pilot lines support the transfer of new technologies from the scientific and laboratory environment to an industrial environment bridging the "Valley of Death" to industrialization.

**EuroPAT-MASIP**[15] demonstrated the importance for Europe to develop an effective pilot line on Fan-Out Wafer Level Packaging (FOWLP) as an essential technology for heterogeneous integration of power electronics for a very diverse set of applications (from imagers to automotive electronics, through radars). Europe has little assembly and packaging capabilities as Asia leads in standard packaging. This pilot line demonstrated that it is possible to be competitive in advanced packaging and that is important to keep Europe competitive in microelectronics.

**APPLAUSE**[16] (Innovation Action though not a pilot line as such) develops specific high-value equipment for the heterogeneous integration of photonic components in an industrial environment, equipment that can be of use in a wide variety of other domains in heterogeneous integration.

**InForMed, Position-II and Moore4Medical** are a suit of pilot lines that realised the first pan-European infrastructure for manufacturing and assembly of small to medium volume of micro-fabricated medical devices in a complete innovation value chain from technology concept to high-volume production and system qualification. InForMed worked amongst other on advanced coating technologies for Bio-MEMS, POSITION-II on advanced Flex-to-Rigid technology, special sensors, etc. resulting in the smart catheter product. Moore4Medical implemented the **open-access offerings to the platforms**, which are being developed like multi-project runs in the semiconductor industry, expanding the technologies to microfluidics, organ-on-chip, silicon pump technology, etc. This environment is well suited to help start-ups launch innovative projects. Open technology platforms for specific domains are economically feasible, only if those platforms are conceived that they can also serve other application domains.

**Photonics pilot lines**

A new and promising field are photonic integrated chips. These devices integrate optical functions and optionally combine them with electronic function. The manufacturing volume is expected to grow significantly over the next years, making industrial exploitation viable (See for example Yole market report on Silicon Photonics[17]. European RTOs have developed state-of-the-art pilot lines for several technology platforms and are capable of low volume manufacturing. But industrial capacity is largely missing so far. The photonics21 partnership has under Horizon2020 supported following pilot lines which helped to get technologies closer to industrial level. These pilot lines are each distributed over several research centres and universities in Europe. In some cases companies which pioneer specific technologies also participate.

[14] https://microprince.eu/
[15] https://www.europat-masip.eu/
[16] https://applause-ecsel.eu/
[17] Silicon Photonics 2021 Market & Technology Report by Yole Développement (i-micronews.com)

Certain device types such as light sources are simpler to realise on Indium-Phosphide wafers (instead of Silicon). The project **InPULSE** strives to bring processing technologies closer to industrial maturity and establishes a platform to build chips which find applications in telecommunication and health[18].

The material Silicon Nitride allows the manipulation of visible light in wave guides with very low losses. This brings advantages for the miniaturisation of sensors for the health and food sector. The project **PIX4Life** has developed a platform for Silicon Photonics chips based on Silicon nitride[19].

Sensors and imaging systems working in the mid-infrared range of light are ideal to detect gases with high very high precision and sensitivity. The Pilot line project **MIRPHAB** has developed technologies to package the relevant optical and electronic components in an package ('system in package') and offers a platform to bring these into industrial application[20].

The packaging of integrated circuits with optical functions is very complex and in need of modularization and standardization to bring down costs and increase reliability. The pilot line project **PIXAPP** has been working on a system platform that makes it simpler for industrial users to pick and tailor processes to their needs[21].

Other projects have established research pilot lines to improve the manufacturing of micro-lenses[22], medical components using light technologies[23] and organic LEDs on flexible substrates[24]. The challenge for all pilot projects is to make the step to high-volume manufacturing which requires buy-in and investment of industrial partners. R&I measures are envisaged under this Act which should help to bridge the gap to industrial uptake.

**Graphene pilot line**

The 2D-EPL project has established a pilot line for prototype production of graphene and related materials (GRM) based electronics, photonics and sensors, based around prototyping services (in the form of Multi Project Wafer runs as well as tailor designed integrations) for 150- and 200-mm wafers, based on the current state-of-the-art graphene device manufacturing and integration techniques. This will ensure external users and customers are served by the 2D-EPL early in the project and guarantees the inclusion of their input in the development of the final processes by providing the specifications on required device layouts, materials and device performances. The consortium will develop a fully automated process flow on 200- and 300-mm wafers, including the growth and transfer of high crystal quality graphene and TMDCs. The project will cover the whole value chain including tool manufacturers, chemical and material providers and pilot lines, to secure progress in GRM integration and to be able to offer prototyping services to academics, SMEs and companies which can benefit from the progresses of GRM integration with silicon achieved within the 2D-EPL consortium.

[18] InPulse - JePPIX Pilot Line - SMART Photonics

[19] Silicon Nitride Photonic Integrated Circuit Pilot line for Life Science Applications in the Visible Range | PIX4LIFE Project

[20] Home - Mirphab

[21] Packaging Solutions - Pixapp

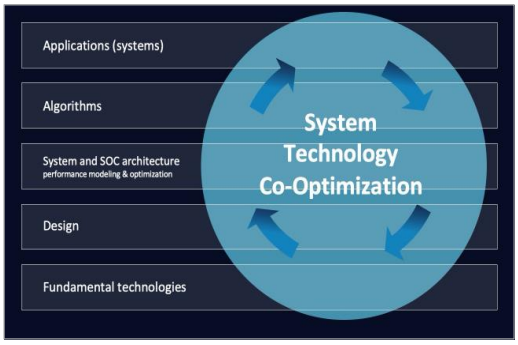
[22] PHABULOuS Pilot Line for free-form micro-optics

[23] Home | Medphab

[24] Lyteus

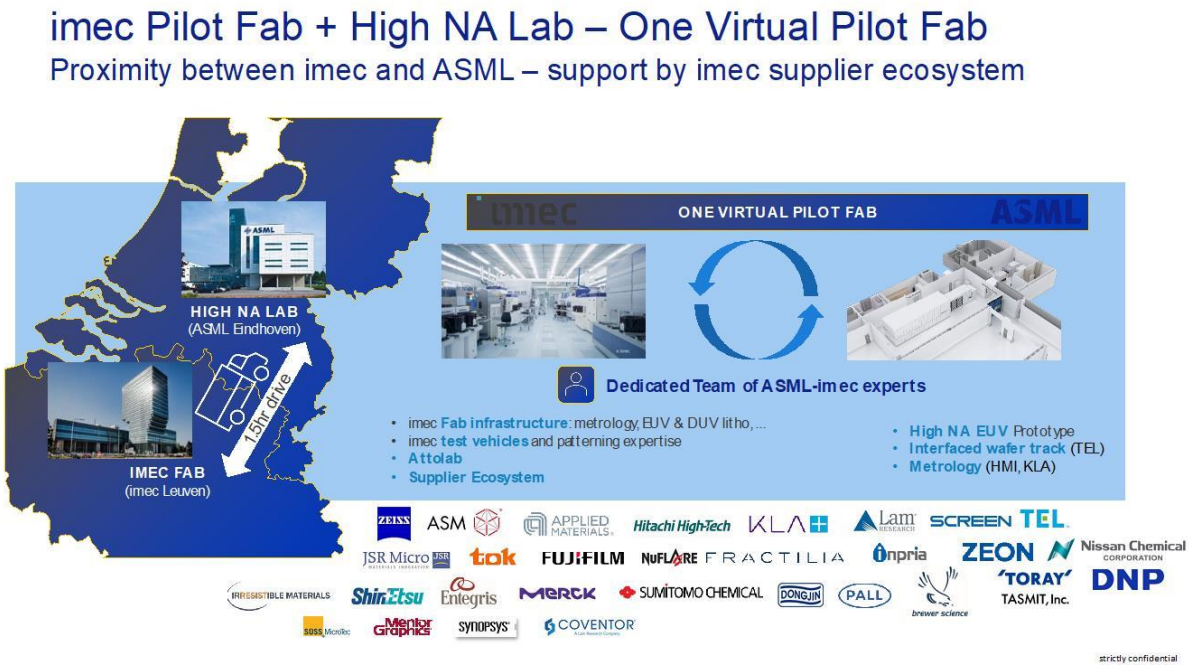
# Annex 6. Chips for Europe: Examples of impact of Pilot Lines

More than ever, equipment & material suppliers are playing a key role in collectively tackling the scaling challenges posed by today's fast-evolving, capital equipment-intensive, complex semiconductor landscape. Strong R&D interactions between manufacturers and suppliers at an early stage of development accelerate technology advancements and optimize the return on investment for all partners involved. The close partnership with leading systems and application companies fuels the methodology of design & system co-optimization, that is key to the multi-domain and multi-scale innovation power brought by **advanced pilot lines facilities**.



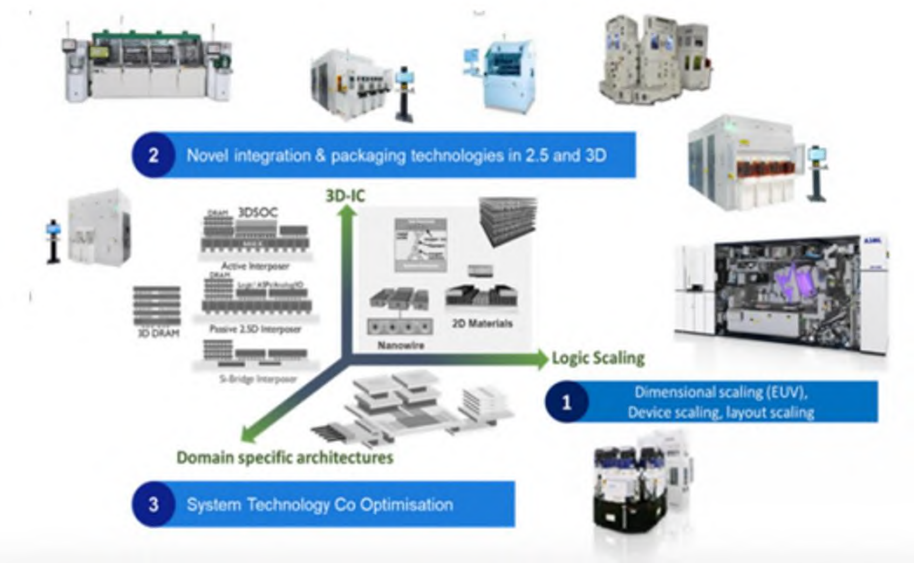

Example #1: The Suppliers' hub

The Chips for Europe's key asset for the European Materials and Equipment suppliers is the suppliers' hub infrastructure. One example is the High-NA EUV research from imec in partnership with ASML. This research is unique in the world and its results will be essential for implementing advanced node logic and memory innovation. Another example is the development of Atomic Layer Deposition, which has become the world standard for deposition of high-k dielectrics and metal gates, and which has been pioneered through early European collaboration of ASM and imec.




Bringing together advanced equipment and materials manufacturers in **a pre-competitive processing facility** offers the opportunity to perform the pathfinding for the process module options of the next-generation technology nodes mentioned above as well as for equipment and materials manufacturers to gain early feedback on their product roadmaps. The imec suppliers' hub, including the ASML partnership, is exemplary for the success of this operational model. A similar hub to support FD-SOI technology at CEA-Leti is also a clear example.

The European suppliers' hub will be a facility that is unique in the world for demonstration and integration of new process modules and that strengthens the European leadership in critical process steps, such as leading-edge lithography, 3D integration, materials, wafer technologies and metrology, sustainability, automation etc. The availability of an extended facility, which allows the individual process modules to become part of a full flow, at appropriate integration density, is of extreme importance to validate the process options and intellectual property valuation.




Leading equipment and materials suppliers can only optimize their tool performance by performing high-value module validation using an industry-relevant pilot line setting, requiring access to the most advanced leading-edge process modules. They achieve this validation by participating in individual innovation programs embedded in an industry-relevant R&D facility, providing the necessary feedback during the equipment development cycle.

Example #2: Exploring the impact of Backside Power Distribution Network on high performance chips

The goal of a power delivery network of a chip is to provide power as well as a reference voltage to the active devices on the die. This network is essentially a network of interconnects that is separate from the signal network. Traditionally, both networks are fabricated through back-end-of-line (BEOL) processing on the frontside of the wafer. But we can also choose to move the power distribution to the backside of the silicon wafer, which today serves only as a carrier. This would allow direct power delivery to the standard cells, and promises to enhance system performance, increase chip area utilization, and reduce BEOL complexity.

ARM, in collaboration with imec, earlier showed the beneficial impact of using backside power delivery as a scaling booster in the design of a central processing unit (CPU). Using backside power delivery turned out to be the most efficient way of delivering power to the circuits. ARM and imec implemented a Cortex A53 CPU design using a future 3-nanometer process developed by imec. It largely improves on the supply-voltage drop that is caused by the resistance in the BEOL of

traditional designs. In the 'winning' processor design, the backside power delivery is connected to a buried power rail, a structural scaling booster in the form of a local power rail that is buried in the chip's front-end-of-line. (https://spectrum.ieee.org/arm-shows-backside-power-delivery-as-path-to-further-moores-law )

However, the realization of true backside power delivery networks comes with additional technological complexities, that are tackled at the pilot line facility. A dedicated wafer thinning process is needed in combination with the ability to process nano-through-silicon-vias that electrically connect the backside to the frontside of the device wafer. The work in imec's pilot line showed progress in developing the critical technology building blocks needed for realizing backside power delivery networks as a structural scaling booster to further the path of Moore's Law. Furthermore, it has been shown that the wafer's backside can create a very dynamic design space with new design options to optimize the power delivery for scaled systems. A perfect example of where a system-technology co-optimization (STCO) will bring very exciting new perspectives for high-performance systems.

This is an interesting example of how new modules can make a difference in system performance, but it requires however to set up the virtual prototype facility to allow for meaningful experiments. In the last section of this document, we explain the flow and characteristics of a professional virtual prototyping infrastructure that will be provided by the Chips for Europe initiative.

Example #3: embedded non-volatile memories for IoT and edge AI

Intrinsic Semiconductor Technologies Ltd ("Intrinsic") has successfully scaled its silicon oxide-based resistive random access memory devices (RRAM) and **demonstrated electrical performance characteristics that will enable their use as high-performance, low-cost, embedded, non-volatile memory in logic devices at advanced processing nodes on imec's pilot line**.

Together with imec, Intrinsic's RRAM devices have been successfully scaled to dimensions of 50 nanometres and have demonstrated excellent switching behavior, which is key to their use as the next generation of non-volatile, solid-state memory. This milestone confirms that the devices are compatible with the advanced semiconductor manufacturing process nodes used across the semiconductor industry, both in terms of physical dimensions (scaling) and electrical performance characteristics, making them suitable for use in Edge AI and IoT applications.

According to Nigel Toon, advisor to Intrinsic and CEO, Graphcore: "Intrinsic is on track to offer a new, embedded, non-volatile memory that is compatible with the most advanced semiconductor process nodes, an option that doesn't exist today.

https://www.semiconductor-digest.com/intrinsic-announces-breakthrough-as-memory-devices-successfully-demonstrated-at-commercially-relevant-nanometre-scale/

Example #4: Europe can become a leader in microdisplays for the ER/VR era

On March 22, 2022 MICLEDI Microdisplays announced an agreement with GlobalFoundries to Collaborate on MicroLED Displays for AR Glasses. MICLEDI Microdisplays, a 2020 spin-off from imec, develops microLED displays for next generation Augmented Reality (AR) glasses. MICLEDI's vision is to enable AR for everyday personal use - smart glasses that are small, lightweight, with long battery life, and at reasonable cost. To make this happen, MICLEDI is developing the world smallest

and brightest displays. The key innovation behind MICLEDI is the **new integration technology for microLED on 300mm wafers developed in the pilot line facility with imec.**

MICLEDI Microdisplays, a leading developer of microLED arrays for augmented reality glasses, today announced a manufacturing collaboration with GlobalFoundries (GF) to enable AR glasses to achieve the brightness, resolution, power, size, and economies of scale needed to be attractive to mainstream consumers. Under the agreement, MICLEDI's solution will be combined with GF's 22FDX® feature-rich platform that provides the leadership performance, ultra-low power and broad feature integration capability needed to build MICLEDI's microLED arrays in mass production. Such companion integrated circuits (ICs), which can be customized for different customer applications, will provide the image processing, driver and control functions needed to complete the display modules using wafer-to-wafer hybrid bonding.

"We are pleased to collaborate with GF as we move from pilot-line manufacturing to mass production in a world-class fab," said Sean Lord, CEO at MICLEDI Microdisplays. "To enable optimum microdisplays for AR, MICLEDI has developed a unique and innovative solution for microLED manufacturing integrating both the controller IC and emitter module to leverage GFs 300mm semiconductor manufacturing technology, capitalizing on manufacturing precision for product performance, high volume and low-cost."

https://www.micledi.com/news/press-release-jan-9th-2020

https://www.micledi.com/news/press-release-march-22nd-2022

Example #5: A technology highly specialized technology module can make all the difference: Hyperspectral imaging

With the advent of more compact hyperspectral cameras and real-time hyperspectral imaging, a set of new applications comes to light. Some examples:

- **agriculture** – Often mounted on drones, light-weight hyperspectral cameras can detect the smallest differences in plants or soils and inform farmers and researchers about diseases, droughts, and so on.
- **machine vision** – Automated industrial processes such as classification, error detection and sorting benefit from a technology that can clearly and quickly distinguish superficially identical entities.
- **medicine** – Thanks to real-time hyperspectral imaging, it's now possible to use hyper-spectral imaging to inspect living tissue, for instance in diagnostic tools or during surgery.
- **art and heritage** – Historical artefacts have many stories to tell. The challenge is to uncover their secrets without touching, and sometimes even moving them. That's where portable, high-resolution hyperspectral cameras come in.
- **remote sensing** – More and more observational satellites leave for space with a hyperspectral sensor on board. It enables them to make out the spectral signatures of soil, vegetation and mineral.
- **forensics** – Hyperspectral imaging's ability to detect spectral fingerprints includes those of materials such as blood or gun powder. It identifies such markers at a crime scene without using chemicals that could tamper with the evidence.

The imec hyperspectral technology has been licensed to the imec spin-off Spectricity, which is a fabless company creating spectral sensing solutions for high-volume and mobile devices, using

CMOS technologies. After the phase of pilot line low volume manufacturing, the company is now looking at doing its test production in a European speciality foundry.

*Example: Machine vision*

In just three years, French company Tridimeo produced a highly precise 3D vision solution for industrial robots. The solution is three times faster than the current industry standard and gives precise "sight" to robots, thereby improving quality checks, picking, and placing parts in challenging lighting conditions. Tridimeo combines 3D and multispectral capabilities to equip manufacturing robots with a robust and reliable set of eyes. The company uses imec multispectral sensors for their solution. **Imec assists in ramping up the production of the sensor now that the start-up company shifts to deployment on an industrial scale.** Renault is Tridimeo's first customer.

Example #6: Specialty components for specific high value – low volume markets

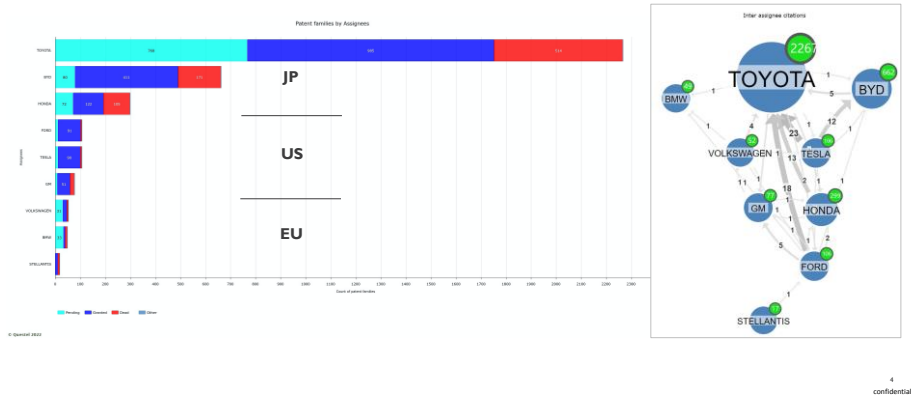
In 2011, Imec announced that it successfully qualified a chipset consisting of custom high-quality EUV sensor dies. These are now being integrated in ASML's NXE:3100 EUV lithography tools in the field, improving the tools' overlay and critical dimension tool performance. The sensors were processed according to ASML's custom designs and specifications, with focus on superior lifetime and sensitivity to direct and high EUV irradiation doses. Two of the sensors are designed to calibrate, align, and focus tool's lens systems. A third sensor is designed to monitor the NXE:3300's EUV dose.

This example confirms that an advanced pilot line can be capable to provide partners with custom specialty chip solutions. Indeed, **a pilot line can offer companies all the services needed to turn innovative ideas into smart packaged microsystem solutions with a wide variety of device technologies** (e.g. CMOS, Si-photonics, MEMS, image sensors, packaging ...). The applications include strategic areas such as bio-sensing, energy- and power management, and high-end specialty imaging, photolithography among others. The pilot line services can range from feasibility studies over design and technology development to prototyping and low-volume manufacturing. And through a strong alliance with the existing foundry and IDM landscape, technology transfer will enable volume production in line with the market demand.

Example #7: IP 'opportunity' in the Automotive

A first analysis of intellectual property creation classified under "semiconductor" in Automotive companies over the period 2010-2020 shows very interesting statistics. The left figure shows the number of semiconductor patent filings by the three largest automotive companies in terms of market cap in Asia, the U.S. and Europe. The right graph shows to which extent the selected patents serve as prior art for each other.

Toyota has filed many patents on semiconductors and further analysis will need to detail the underlying patent family streams but an early start on electrification is most certainly an underlying aspect. Toyota is clearly a technology leader as their patents are prior art for many automotive companies. While the sheer size of Toyota's patent portfolio certainly drives this result, it is apparent that for 1 out of 5 patents by Tesla or Ford a Toyota patent is prior art, while this is barely the case for EU automotive companies, indicating that the technology portfolios of U.S. automotive companies are closer to Toyota than the technology portfolios of EU automotive companies.




*Notes: The graphs show patents with a priority date between 2010 and 2020 that are classified under the International Patent Classification H01L (~semiconductor devices).*

The U.S. automotive companies come behind Asia but before Europe in semiconductor patent activity. This ranking holds both in the absolute number of patent filings, as well as in relative numbers when we look at the ratio of semiconductor patent filings to total patent filings by automotive companies. When looking at filing trends over time, it is noticeable that there is an uptake in Ford's semiconductor patents from 2015 onwards, while at European companies the uptake in semiconductor patents is less outspoken. European car manufacturers clearly have another strategy since they are relatively absent on the patenting scene in this category and probably largely rely on their Tier-1 and Tier-2 suppliers for semiconductor innovations. While this has worked in the past when semiconductors were less central in the innovation of automotive – though were essential in differentiating functions such as safety features, microcontrollers and various sensing and imaging functions and of course entertainment – the future is different. The car will be an HPC cluster on wheels with the semiconductor innovation at the heart.

**The pilot line facility can help to innovate through the full stack of the ecosystem and provide winning intellectual property** to the automotive industry in leading-edge technologies through virtual prototyping and early system impact innovation.

Example #8: Next Generation Communications Infrastructure

As stated by Alexandros Kaloxylos, Executive Director of 6G-IA, "The role of micro-electronics in the evolution of telecommunication networks and services is undeniable. As Europe should keep its leading position in telecommunications, the impact of microelectronics in the ICT sector is of prime concern for the members of the 6G-IA. Thus, it is vital to identify future telecommunication networks' technologies and their requirements from the underlying hardware infrastructure."

An ongoing roadmapping exercise (CoreNect) with partners from across the telecommunications industry such as Nokia, Ericsson, NXP and ST clearly states that with its strong position in the infrastructure market and research, its expertise in material science, and the existing fabrication capacity, Europe could become an IC design and fabrication powerhouse. However, it is repeatedly mentioned that the packaging level will require advanced PCB technology or heterogeneous 2.5D / 3D integration. As several European companies and research groups (among which the large RTOs

imec, CEALeti and Fraunhofer) are strong in this domain, a transfer of this know-how to the industry is an opportunity for Europe to play a stronger and critical role at a higher level in the supply chain than solely at the level of chip design and processing. This is an area where virtual prototyping and early access to pilot lines are key to prove out the co-design of technologies.

A first example from the wireless space is in the mobile network's energy of which 80% is consumed by base station sites. In particular, the composing chipsets. or systems-on-chips (SoC), are major contributors to the energy consumption. The base station systems for beyond 5G hence need to be highly energy efficient on the one hand, but on the other hand they also need to handle extremely high data rates, should not introduce high processing latency and provide sufficient flexibility for features like dynamic spectrum sharing. (https://www.bell-labs.com/collaboration-opportunities/d-a-p/collaborations-ku-leuven-and-imec-push-state-art-energy/). Together with imec, Nokia Bell Labs have developed a novel way to partition the SoC's on-chip memory system and to drastically reduce the energy consumption. In order to achieve an optimal partitioned architecture, we have devised a simulation platform that allows a fast design-space exploration.

A second example is the collaboration with CST Global on disruptive, integrated silicon photonics systems which benefitted from early access to a pilot line-like technology. Anders Storm, CEO of Sivers IMA, said, "The integration of imec's advanced SiPho technology platform with our indium phosphide (InP) DFB lasers and InP reflective semiconductor optical amplifier (RSOA) Photonics solutions, has already demonstrated excellent results. We expect that these new light sources will encourage the uptake of SiPho devices in a wider range of cost-sensitive, industrial markets. The collaboration between the exceptional design and manufacturing team at our Photonics unit, CST Global, in Glasgow, UK and imec's world-leading research and innovation hub in nanoelectronics and digital technologies, will allow the creation of disruptive, integrated SiPho systems with superior performance and reduced cost." (04/03/2020)

In general, it is expected that next-generation wireless and wireline communication systems will bank on a combination of both very high speed, highly scaled digital nodes and novel material systems. A design infrastructure which combines virtual prototyping with a pilot line to verify the critical differentiation steps for European technology integration would multiply opportunities as shown above.

Example #9: supporting innovations through realization of companies ASIC ideas. (EUROPRACTICE example)

Wiyo is a Spanish Internet of things (IoT) start-up that created an intelligent tag to enable simple and efficient solutions in the world of automatic identification and data capture. When you put the Wiyo solution in any object or physical element, you can immediately interact with, sense, and follow that object in real time – regardless of whether it's moving or stable. Consider it an RTLS (real-time location system) and IoE (Internet of Everything) solution without a battery and with no dedicated readers. Any generic Wi-Fi source can power and enable the interaction. The solution has countless possibilities and lots of industries can take advantage of it (smart hospitals, smart stores, smart food deliveries, Industry 4.0, ...). When it became clear that this solution needed a chip, Wiyo contacted the imec.IC-link team that gave support/advise throughout the whole flow of the ASIC development from technology choice up to building the capacity to test the chip, improving the design for future manufacturing, and adding design for testing to get ready for mass production.

(https://www.imeciclink.com/en/articles/start-doesnt-have-time-or-money-make-mistakes)

Turning company ASIC ideas into real products can be a complex process. By utilizing its partner network, imec.IC-link offers a complete range – from ASIC design to product qualification (use of EDA tools, technology and design support, standard packaging for test chips and extensive training). Once the company is ready to fabricate its ASIC design, Imec.IC-link assists with flexible access to multi-project wafer (MPW) and volume production at leading foundries for mature and advanced nodes, including its own innovative technologies such as gallium nitride and silicon photonics.

It is expected that the technology in the next decade will be even more complex than it is today and as such the way of working that is in place at imec.IC-link is seen as a good starting point for attracting and supporting customers of the pilot lines.

Example #10: supporting the industry in the area of Fan-Out Wafer Level Packaging

Heterogeneous integration is one of the most promising ways to bridge the gap between emerging microelectronics and its derived applications, both are pushing new packaging technologies. New technology architectures are needed to integrate the progress made in nano-electronics, wireless technologies and photonic component technologies into electronic systems. Fan-out wafer level packaging (FO-WLP) or panel level packaging (FO-PLP) is now the optimal result of the merge between single-chip and multi-chip packages. The evolution of single chip packages (SCPs) has started from small metal boxes and developed for dual inline packaging (DIP) for through-hole assembly and surface mount technology (SMT) packages such as the quad flat package (QFP) to the ball grid array (BGA). BGA packages use rigid or flexible interposer for the redistribution from the peripheral pads to the area array. The minimum packages size has been achieved with WLP because the package size is equal to the die size. For all these packages OSATs are needed for SMEs. Due to the nature of standardized packages even small companies and R&D institutes are supported in this are by small volume offers. Further advanced packages are based on embedding technology. The main advantages of FO-WLP and FO-PLP are the substrate-less package, lower thermal resistance, higher performance due to shorter interconnects together with direct IC connection by thin film metallization instead of wire bonds or flip chip bumps and lower parasitic effects. Especially the inductance of FO-WLP is much lower compared to FC-BGA packages. In addition, the redistribution layer can also provide embedded passives (R, L, C) as well as antenna structures using a multi-layer structure. Therefore, FO-WLP are used for multi-chip packages and can be viewed as a synergy between optimal chip package and the MCM concepts. Hence, technology is well suited for heterogeneous integration which is only possible on wafer or panel scale. Unfortunately, small volumes are not offered by OSATs due to wafer or panel scale fabrication. Therefore, a multi-project approach is extremely needed to open the advantages of these packages also for SMEs.

Fraunhofer has started an international consortium to explore the potential of this technology. After the international Panel Level Consortium 1.0 has achieved the overall goals of the project in 2019 with significant technical progress in the field of large area Fan-out Panel Level Packaging a new consortium has been formed to continue the development with a focus on ultra fine-line routing including R&D on migration effects. The project has started 1st of February 2020 and will run for two years. Partner which have signed for the consortium up to now are: Ajinomoto Group, Amkor Technology, ASM Pacific Technology Ltd., AT&S Austria Technologie & Systemtechnik AG, BASF, Corning Research & Development Corporation, Dupont, Evatec AG, FUJIFILM Electronic Materials U.S.A., Hitachi Chemical Company, Ltd., Intel Corporation, Meltex Inc., Nagase, RENA Technologies GmbH, Schmoll Maschinen and Semsysco GmbH.

Example #11: High density interconnect for highest bandwidth at lowest power

Future electronic systems like autonomous systems using high performance computing (HPC) and edge computing systems, sensor integrated systems and bio-integrated devices will require more and more functions which cannot be managed by a single chip, even if advanced SoC (System on Chip) concepts are used. Heterogeneous integration will be the next step and will pass beyond current SiP (System in Package) approaches.

A main bottleneck is the efficiency of data handling between computational processing units and memories. As an example today's supercomputers run at about 5% or even less of their theoretical computing power due to the limited memory bandwidth New hardware and software architectures are necessary to break down the boundary between pure logic and pure memory domains. One very suitable approach hereby is the split up of the different logic building blocks into chiplets. In that way, the connections can be optimized in respect to increase bandwidth bottlenecks. Furthermore, the yield of very complex processing units results in extreme increasing costs alongside with further front end node miniaturization in the IC manufacturing process. This can be overcome by the use of chiplets which means that IP blocks made in different technology nodes will be combined on an interposer to reduce cost by increasing the production yield (smaller chips) and reuse across applications. Different technology options are possible for routing the high density lines on the substrate: Si-Interposers are already proven as a possible but high-cost solution, high density organic substrates with or without embedding technologies and the different variations of Fan-Out packaging approaches using molded substrates with embedded active components. With the emerge of sub-7nm technologies, also the need to merge CMOS cores with non-CMOS technology will become necessary for cost and performance reasons in medium term, increasingly. Therefore, the concept of chiplets which split such difficult-to-make functional blocks into modules that are more manageable, will mainly benefit from this new interconnection technologies.

In short-term heterogeneous integration will appear at chip, package and organic substrate or panel level. The main physical advantages are the lower thermal resistance, higher performance making it ideally suited for RF applications like 5G and beyond. Extreme high density interconnect approaches such as hybrid bonding in combination with TSVs push the limits regarding CMP-capability in back end and placement accuracy with the potential to replace microbump flip-chip assembly in long-term for highest performance applications. Therefore, the development and standardization of active Si-interposer concepts using hybrid bonding for chiplets using sub 1 µm interconnection precision is necessary for electrical and physical interface standards for data rates into the TB/s regime with energy efficiencies down to 0,2pJ/bit and ns latency for high performance computing. Future electronic systems will be based on increased functionality requiring not only the integration of different technologies but also optimization with respect to reduced carbon footprint and low energy consumption. Highest reliability and long lifetime for autonomous systems will be key for economic success keeping an optimized balance between cost and performance. Hardware /software co-designs must be the result as an Assembly Design Kit (ADK) for new complex packages like wafer and panel level embedding for further miniaturization, enhanced functionality, and increased energy efficiency. Looking on the technological variety and their demands for high performance applications, there will be a significant impact on the package supply chain in the industry. Whereas strict separation of front end, OSAT and substrate suppliers dominated the past, these boundaries seem to vanish more and more as the need for miniaturization to keep up with Moore's law cannot be fulfilled by node miniaturization alone and will be distributed alongside the supply chain. This is especially valid for packages in the field of high performance applications like IoT and edge devices in the era of AI.

Example #12: Exploring the Green Potential of New Advanced Packages

Packaging of electronic components is often considered a small addition to the manufacturing of the core functionality of the component. In particular, for semiconductors, or integrated circuits (ICs), the majority of investments, developments and personnel will be focused on manufacturing the highest performing chips with the smallest reproducible features in huge cleanroom facilities. Packaging, on the other hand, is not core business and has typically been outsourced or shifted away to former low wage countries in Asia, such as the Philippines or Malaysia . Conventionally, the cost of packaging is only a few percent of the component costs, and likewise – though few studies reveal data publicly – packaging will only contribute a few percent to the environmental profile of a component. Current research in the field of environmental assessment and cost modeling of microelectronic manufacturing indicates that with advanced packaging technologies and the prominent example of chiplets, the value contribution of packaging increases and in some cases can suddenly contribute dominant effects. These effects would appear both in economic analysis and environmental impacts. The implications are two-fold: chiplets could deliver substantial improvements (i.e. lower impacts for same or higher functionality), but could also introduce new critical materials and increase environmental impacts per delivered functionality.

In summary, a new IC packaging paradigm introduces new processing steps and new materials in the production stage in order to drive miniaturization and performance forward, while keeping the costs balanced to the performance gains. Therefore, on the one hand, environmental analysis on an in-depth technical level is needed to determine the environmental effects of introducing a new packaging technology, such as chiplets. On the other hand, we need to make sure that environmental practitioners identify and assess multi-chip packages correctly to begin with.

Example #13: Packaging DfR (Design-for-Reliability) Toolbox

The Vision:

Mission profile adapted functional product qualification

Standardised common mission profiles

Structured database of characterised available technologies and models

Why does the industry need a DfR Toolbox now?

Shortening product cycles and shortening of development times

Extended lifetime requirements (i.e. automobile electrification)

Diversity of application and packaging scenarios (IOT, 5G, Robotics, …)

Use of COTS in Non-Consumer application (need for requalification)

Increasing sensitivity of consumers (i.e. Premature Obsolescence)

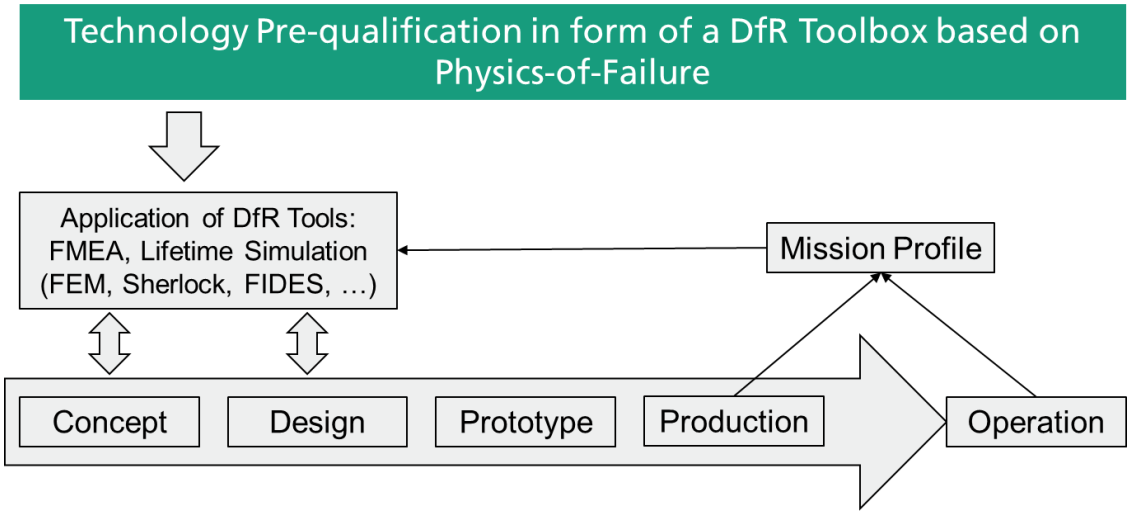
Outcome

Early access to know-how on leading-edge technology robustness

Special technology lifetime models

Acceleration factors / activation energies and validation of lifetime models

Models for early design evaluation usable in design tools (e.g. Sherlock)




How Virtual Prototyping on the pilot lines works

The goal of designing a virtual prototype is to explore system-level impact of the proposed innovative semiconductor integration technology and manufacturing options at component and IP-block level, at system-on-a-chip level or even at board or blade level.

In this context, the design is implemented using infrastructure that consists of the PDKs (process design kits) and EDA (electronic design automation) flows that represent the proposed innovative semiconductor integration technology and manufacturing options.

The virtual prototype then allows a validation of the value proposition and trade-offs in terms of materials, device, design, and architecture options.

This requires that the PDKs are mature enough to support the complete design flow from RTL to GDS. The design infrastructure must be complete enough to evaluate PPAC at a level that shows non-trivial impact and complex ROI calculation of basic innovation questions. The digital part of a PDK has many hundreds of cells, of which almost all are needed to implement a CPU as well as memory primitives and structure compilers. The design infrastructure includes geometry rules needed to implement significant analogue circuit IP, such as SERDES, PLLs and specialized I/O cells, as well as tools for analogue design, RTL synthesis, logical equivalency, ERC/DRC, etc.

**A pilot line is the enabling manufacturing infrastructure necessary for realizing hardware to calibrate and correlate with the model assumptions.**

There is a very close interaction between the activities executed on the pilot lines and the practice of virtual prototyping. A virtual prototype addresses critical technology-related questions like “Is the device performance meeting expectations?"

Note, this **does not** imply that the entire virtual prototype is “taped-out” in the “pilot line”, but rather identifies critical constituents at the level of a logic gate, or critical process module, or part of integration stack that **informs critical PDK** implementation parameters. These parameters are then

used to finetune the PDK parameters of the virtual prototype creating a feedback loop between virtual prototype and manufactured samples.

Design infrastructure is also a critical piece of the equation. Without design-infrastructure enablement there is no fundamental connection between the complex trade-offs at the level of significant IP architecture and micro-architecture and the technology development and improvements that are achieved in the pilot fab through technology innovation.

These design infrastructure critical skills are required to realize the custom PDKs and implementation extras that are used to implement virtual prototypes and guide the complex DOE (Design of Experiments) trade-offs that are needed in the pilot line. **One cannot minimize the fundamental need for this capability and its tailored nature to a particular technology implementation. More crisply: the skills needed to implement PDKs and virtual prototypes are fundamentally tied to the technology DOEs and have to be part of the same organization.**